

1. (TWICE AMENDED) An apparatus comprising:

a circuit comprising a plurality of inputs configured to provide a selected device identification (ID) from a plurality of different device IDs, wherein said plurality of inputs allow said circuit to be implemented with any of said plurality of different device IDs.

2. (TWICE AMENDED) The apparatus according to claim 1,

wherein said selected device ID comprises a soft code.

3. (AMENDED) The apparatus according to claim 1,

wherein said circuit comprises a JTAG compliant controller.

4. (TWICE AMENDED) The apparatus according to claim 1,

wherein each of said plurality of different device IDs identifies a unique configuration of said circuit.

5. (TWICE AMENDED) The apparatus according to claim 1,

wherein said selected device identification ID can be reconfigured after fabrication of said apparatus.

6. (TWICE AMENDED) The apparatus according to claim 1,

wherein said circuit comprises:

a logic circuit configured to receive said plurality of inputs;

5 a multiplexer configured to receive an output of said logic circuit; and

a memory element configured to receive an output of said multiplexer.

7. The apparatus according to claim 6, wherein said multiplexer is further configured to receive an input signal and a shift signal.

8. The apparatus according to claim 7, wherein said logic circuit comprises a logic gate.

9. (AMENDED) The apparatus according to claim 1, wherein said apparatus further comprises a FIFO memory.

10. (AMENDED) The apparatus according to claim 1, wherein said plurality of inputs comprise mark options.

11. (AMENDED) The apparatus according to claim 1, wherein said plurality of inputs comprise configuration input pins.

12. The apparatus according to claim 1, wherein said circuit comprises a JTAG device compliant with the IEEE standard 1149.1.

13. (TWICE AMENDED) An apparatus comprising:
means for receiving a plurality of inputs; and
means for providing a selected device identification (ID) from a plurality of different device IDs, wherein said plurality of
5 inputs allow implementation of any of said plurality of different device IDs.

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14. (TWICE AMENDED) A method for selecting one of a plurality of different device identifications (IDs) comprising the steps of:

(A) receiving a plurality of inputs configured to select
5 said one of said plurality of different device IDs; and

(B) configuring a device with said selected device identification (ID), wherein said plurality of inputs allow implementation of any of said plurality of different device IDs.

15. (TWICE AMENDED) The method according to claim 14, wherein said selected device ID comprises a soft code.

16. (TWICE AMENDED) The method according to claim 14, wherein each of said different device IDs identifies a unique circuit configuration.

17. (AMENDED) The method according to claim 14, wherein said selected device identification ID can be reconfigured after fabrication.

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18. (AMENDED) The method according to claim 14, wherein said plurality of inputs comprise mark options.

19. (AMENDED) The method according to claim 14, wherein said plurality of inputs comprise configuration input pins.

20. The method according to claim 14, further comprising providing a JTAG device compliant with the IEEE standard 1149.1.
